AN4243
Application note

The L6230 DMOS driver for three-phase brushless DC motor

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Introduction

Modern motion control applications need more flexibility that can be only addressed with specialized ICs products. The L6230 is a DMOS fully integrated three-phase BLDC motor driver optimized for field oriented control (FOC) application thanks to the independent current senses. The device integrates six DMOS power transistors with CMOS and bipolar circuits on the same chip including overcurrent protection for safe operation and flexibility. An uncommitted comparator with open-drain output for optional function is available.

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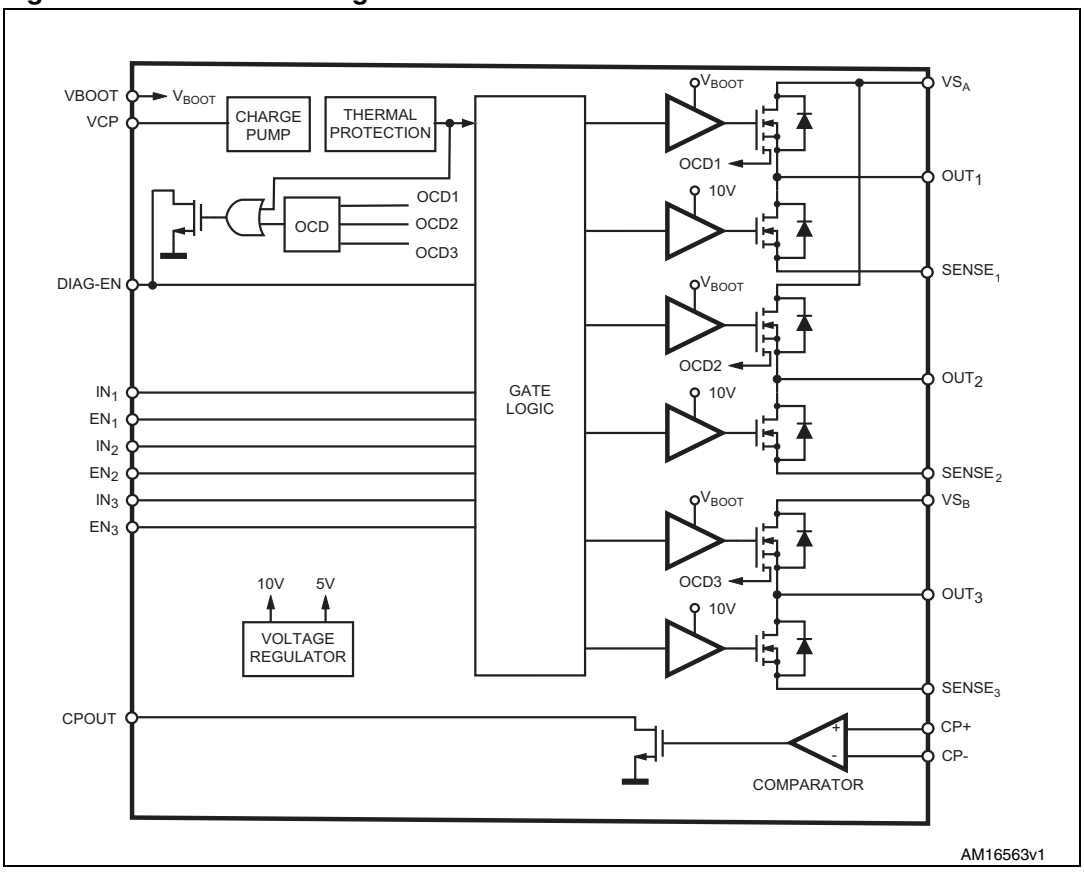
1 L6230 block diagram

The L6230 (see *Figure 1*) includes logic for CMOS/TTL interface, a charge pump that provides auxiliary voltage to drive the high-side DMOS, non-dissipative overcurrent protection circuitry on the high-side DMOS, with a fixed trip point set at 2.8 A (see *Section 2.10*), overtemperature protection, undervoltage lockout for reliable startup.

Figure 1. L6230 block diagram



2 Designing an application with the L6230

2.1 Current ratings

With MOSFET (DMOS) devices, unlike bipolar transistors, the current under short-circuit conditions is, at first approximation, limited by the $R_{DS(on)}$ of the DMOS themselves and could reach very high values.

The L6230 OUT pins and the two V_{SA} and V_{SB} pins are rated for a maximum of 1.4 A r.m.s and 2.8 A peak (typical values). These values are meant to avoid damaging metal structures, including the metallization on the die and bond wires.

In practical applications, maximum allowable current is less than these limits; actually the constraint is the power dissipation. The device integrates overcurrent detection (OCD) that provides protection against short-circuits between the outputs and between an output and ground (see *Section 2.10*).

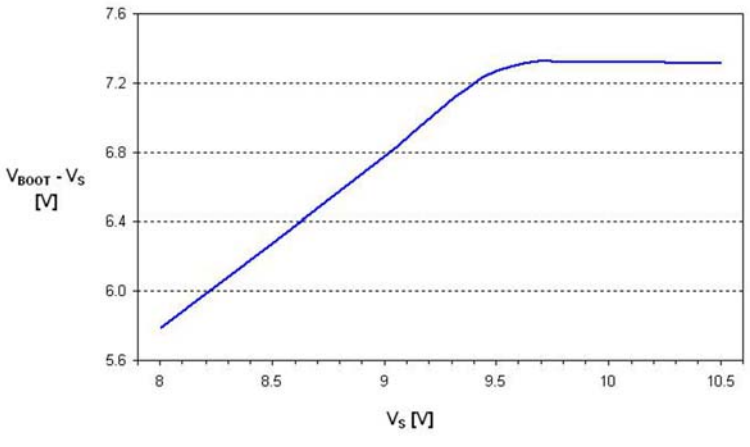
2.2 Voltage ratings and operating range

The L6230 requires a single supply voltage (V_S), for the motor supply. Internal voltage regulators provide the 5 V and 10 V required for the internal circuitry.

The operating range for V_S is from 8 to 52 V. To prevent from working into undesirable low voltage supply an undervoltage lockout (UVLO), circuit shuts down the device when supply voltage falls below 6 V; to resume normal operating conditions, V_S must then exceed 6.8 V. The hysteresis is provided to avoid false intervention of the UVLO function during fast V_S ringings.

It should be noted, however, that DMOS's $R_{DS(on)}$ is a function of the V_S supply voltage. Actually, when V_S is less than 10 V, $R_{DS(on)}$ is adversely affected, and this is particularly true for the high-side DMOS that are driven from VBOOT supply. This supply is obtained through a charge pump from the internal 10 V supply, which tends to reduce its output voltage when V_S goes below 10 V. *Figure 2* shows the supply voltage of the high-side gate drivers (VBOOT - V_S) versus the supply voltage (V_S).

Figure 2. Supply voltage of high-side gate drivers versus supply voltage



Note that V_S must be connected to both V_{SA} and V_{SB} since the bootstrap voltage (at VBOOT pin) is the same as the three half-bridges. The integrated DMOS have a rated drain-source breakdown voltage of 60 V. However V_S should be kept below 52 V, since, in normal working conditions, the DMOS see a V_{ds} voltage that exceeds the V_S supply. In particular, when a high-side DMOS turns off due to a phase change (OUT1 in *Figure 3*), if one of the other outputs (OUT2 in *Figure 3*) is high, the load current starts flowing in the low-side freewheeling diode and the SENSE pin sees a negative spike due to a non-negligible parasitic inductance of the PCB path from the pin to GND. This spike is followed by a stable negative voltage due to the drop on R_{SENSE}. The OUT pin sees a similar behavior, but with a slightly larger voltage due to the forward recovery time of the integrated freewheeling diode and the forward voltage drop across it. Typical duration of this spike is 30 ns. At the same time, the OUT2 pin (in the example of *Figure 3*) sees a voltage above V_S, due to voltage drop across the high-side (integrated) freewheeling diode, as the current reverses direction and flows into the bulk capacitor. It turns out that the highest differential voltage is observed between two OUT pins when a phase change turns a high-side off, and this must always be kept below 60 V.

Figure 3. Currents and voltages if a phase change turns a high-side off during off-time

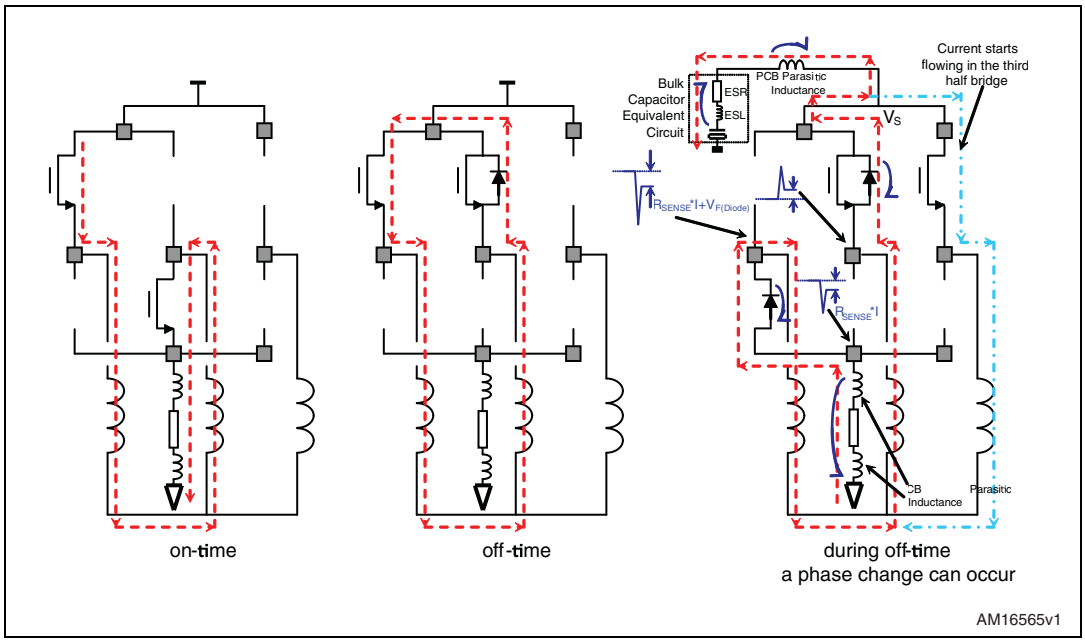
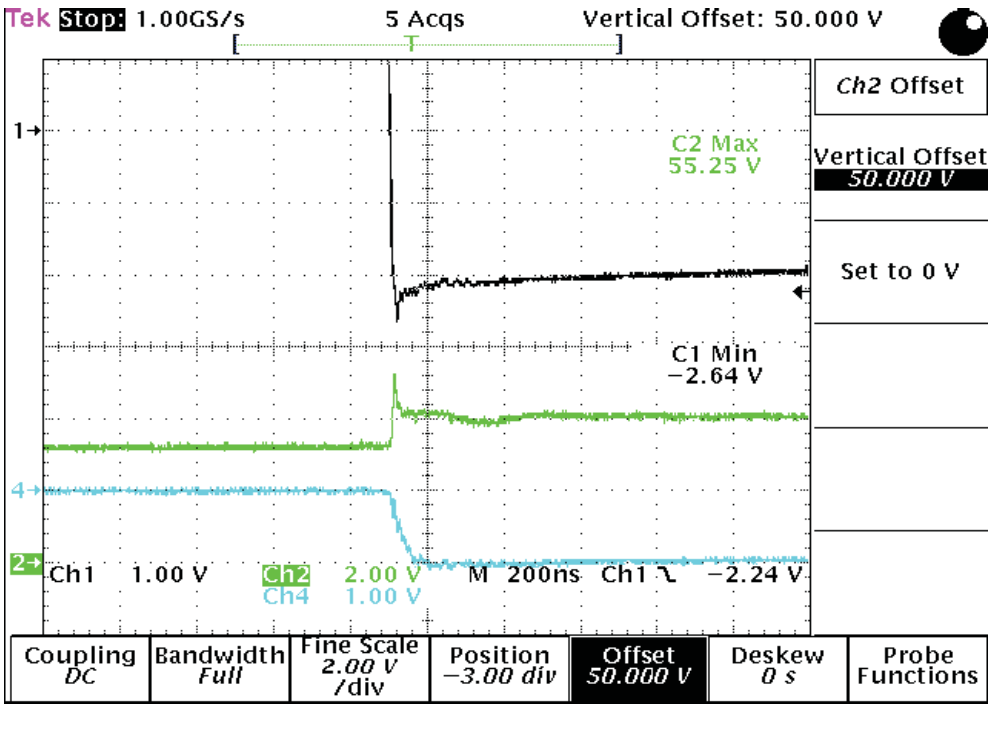


Figure 4 shows the voltage waveforms at the OUT pins referring to a possible practical situation, with a peak output current of 1.4 A, V_S = 52 V, R_{SENSE} = 0.33 Ω, T_J = 25 ºC (approximately) and a good PCB layout.

Below ground spike amplitude is -2.65 V for one output, the other OUT pin is at about 55 V. In these conditions, total differential voltage reaches almost 60 V, which is the absolute maximum rating for the DMOS. Keeping differential voltage between two output pins within rated values is a must that can be accomplished with proper selection of bulk capacitor value and equivalent series resistance (ESR), according to the current peaks and adopting good layout practices to minimize PCB parasitic inductances.

Figure 4. Voltage at the two outputs if a phase change turns a high-side off



2.3 Choosing the bulk capacitor

Since the bulk capacitor, placed between V_S and GND pins, is charged and discharged during IC operation, its AC current capability must be greater than the RMS value of the charge/discharge current. This current flows from the capacitor to the IC during the on-time (t_{ON}) and from the IC (implementing a fast decay current recirculation technique) or from the power supply (implementing a slow decay current recirculation technique) to the capacitor during the off-time (t_{OFF}).

The RMS value of the current flowing into the bulk capacitor depends on peak output current, output current ripple, switching frequency, duty cycle. It also depends on power supply characteristics. A power supply with poor high-frequency performances (or long, inductive connections to the IC) causes the bulk capacitor to be recharged slowly: the higher the current control switching frequency, the higher the current ripple in the capacitor. RMS current in the capacitor, however, does not exceed the RMS output current. Bulk capacitor value (C) and the ESR determine the amount of voltage ripple on the capacitor itself and on the IC.

In slow decay, neglecting the deadtime and output current ripple and assuming that during the on-time the capacitor is not recharged by the power supply, the voltage at the end of the on-time is:

Equation 1

$$V_S - I_{out} \cdot \left(ESR + \frac{t_{on}}{C} \right)$$

so the supply voltage ripple is:

Equation 2

$$V_S - I_{out} \cdot \left(ESR + \frac{t_{on}}{C} \right)$$

where I_{OUT} is the output current.

With fast decay, instead, recirculating current recharges the capacitor, causing the supply voltage to exceed the nominal voltage. This can be very dangerous if the nominal supply voltage is close to the maximum recommended supply voltage (52 V). In fast decay the supply voltage ripple is about:

Equation 3

$$I_{OUT} \cdot \left(2 \cdot \ ESR + \frac{t_{ON} + t_{OFF}}{c} \right)$$

always assuming that the power supply does not recharge the capacitor, and neglecting the output current ripple and the deadtime.

Usually (if C > 100 µF) the capacitance role is much less than the ESR, then supply voltage ripple can be estimated as:

Equation 4

$$I_{OUT} \cdot \ ESR \quad \text{in slow decay}$$

Equation 5

$$I_{OUT} \cdot \ ESR \quad \text{in fast decay}$$

For example, if a maximum ripple of 500 mV is allowed and I_{OUT} = 1 A, the capacitor ESR should be lower than:

Equation 6

$$ESR < \frac{0.5V}{1A} = 500m\Omega \quad \text{in slow decay}$$

Equation 7

$$ESR < \frac{1}{2} \cdot \ \frac{0.5V}{1A} = 250(500)m\Omega \quad \text{in fast decay}$$

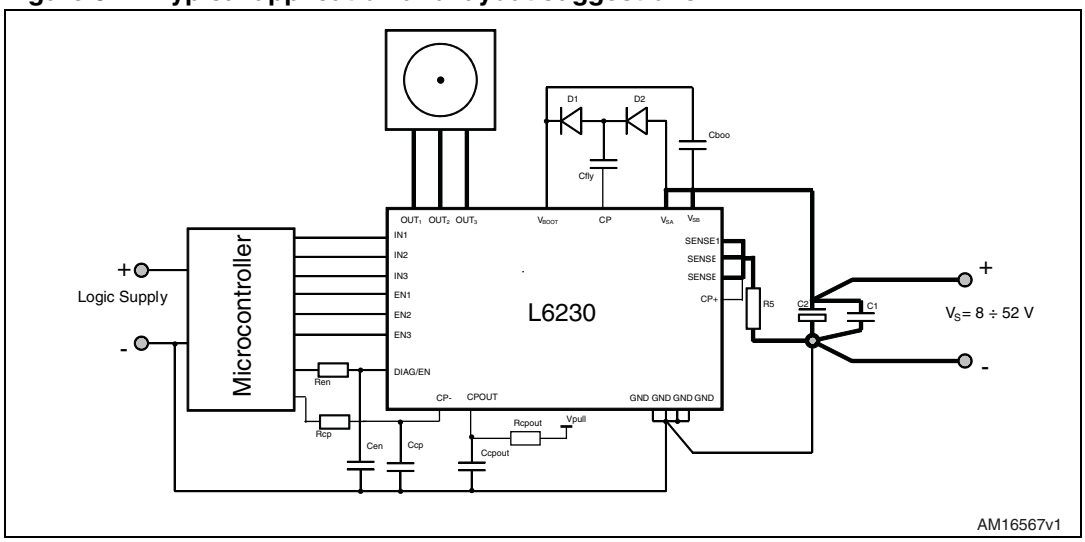
Actually, current, sunk by V_{SA} and V_{SB} pins of the device, is subject to higher peaks due to reverse recovery charge of internal freewheeling diodes. The duration of these peaks is, tough, very short and can be filtered using a small value (100 ÷ 200 nF), good quality ceramic capacitor, connected as close as possible to the V_{SA}, V_{SB} and GND pins of the IC. The bulk capacitor is chosen with maximum operating voltage 25% greater than the maximum supply voltage, considering also power supply tolerances.

For example, with a 48 V nominal power supply, with 5% tolerance, maximum voltage is 50.4 V, then operating voltage for the capacitor should be at least 63 V.

2.4 Layout considerations

Working with devices that combine high power switches and control logic in the same IC, special attention has to be paid to the PCB layout. In extreme cases, Power DMOS commutation can induce noises that could cause improper operation in the logic section of the device. Noise can be radiated by high dV/dt nodes or high dI/dt paths, or conducted through GND or supply connections. Logic connections, especially high-impedance nodes (actually all logic input, see further), must be kept far from switching nodes and paths. With the L6230, in particular, external components for the charge pump circuitry should be connected together through short paths, since these components are subject to voltage and current switching at relatively high frequency (600 kHz). The primary means to minimize conducted noise is to have a good GND layout (see *Figure 5*).

Figure 5. Typical application and layout suggestions



High-current GND tracks (i.e. the tracks connected to the sensing resistor) must be connected directly to the negative terminal of the bulk capacitor. A good quality, high frequency bypass capacitor is also required (typically from 100 nF to 200 nF ceramic would suffice), since electrolytic capacitors show a poor high frequency performance. Both bulk electrolytic and high frequency bypass capacitors have to be connected with short tracks to V_{SA}, V_{SB} and GND.

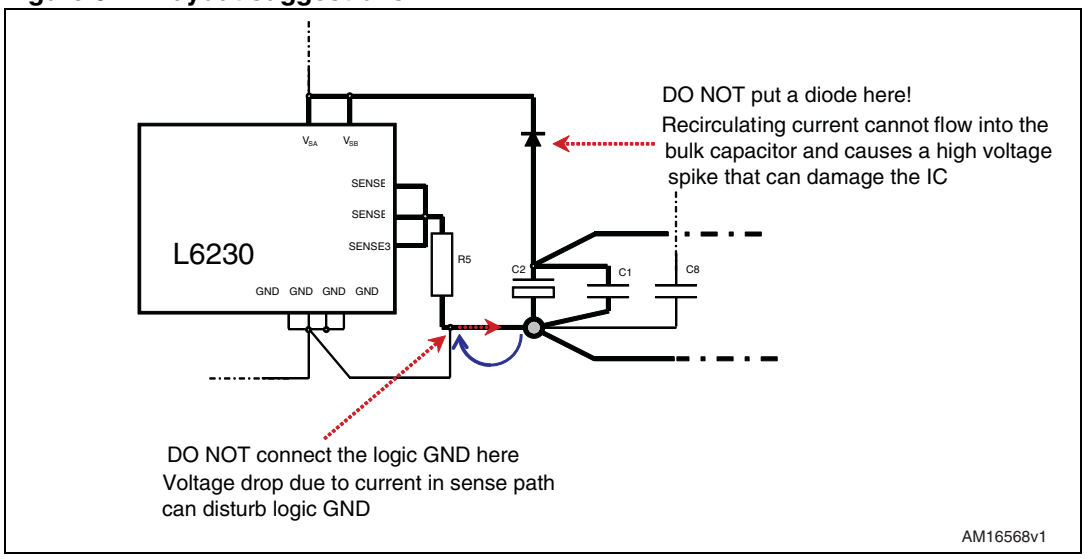
On the L6230, GND pins are the logic ground, since only the quiescent current flows through them. Logic ground and power ground should be connected together in a single point, the bulk capacitor, to avoid the power ground noise from affecting the logic ground. Layouting the path from the SENSE pins through the sensing resistor to the negative terminal of the bulk capacitor (power ground) requires particular attention. These tracks must be as short as possible in order to minimize parasitic inductances that can cause dangerous voltage spikes on SENSE and OUT pins (see *Section 2.2*). For the same reason, the capacitors on V_{SA}, V_{SB} and GND pins should be very close to the GND and supply pins. Refer to the *Section 2.5* for information on selecting the sense resistors. Traces connected to V_{SA}, V_{SB}, SENSEA, SENSEB, and the three OUT pins must be designed with adequate width, since high-currents are flowing through these traces, and layer changes should be

avoided. Should a layer change be necessary, multiple and large via holes have to be used. A wide GND copper area can be used to improve power dissipation for the device.

Figure 6 shows two typical situations that must be avoided. An important consideration about the location of the bulk capacitor is the ability to absorb the inductive energy from the load, without allowing the supply voltage to exceed the maximum rating. The diode shown in *Figure 6* prevents the recirculation current from reaching the capacitors and results in a high voltage on the IC pins that can damage the device.

Having a switch or a power connection that can disconnect the capacitors from the IC, while there is still current in the motor, also results in a high-voltage transient since there is no capacitance to absorb the recirculation current.

Figure 6. Layout suggestions


DO NOT put a diode here!
Recirculating current cannot flow into the bulk capacitor and causes a high voltage spike that can damage the IC
L6230
SENSE
SENSE
SENSE3
GND GND GND GND
R5
C2
C1
C8
DO NOT connect the logic GND here
Voltage drop due to current in sense path can disturb logic GND
AM16568v1

2.5 Sensing resistor

Each motor winding current flows through the sensing resistors, causing a voltage drop that is used to control the peak value of the load current. Two issues must be taken into account when choosing the R_{SENSE} value.

The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason, the resistance of this component should be kept low.

The voltage drop across R_{SENSE} can be compared to a reference voltage. The lower is the R_{SENSE} value, the higher is the peak current error due to noise input and to the input offset of the current sense comparator: too small values of R_{SENSE} must be avoided.

A good compromise is to calculate the sensing resistor value so that the voltage drop, corresponding to the peak current in the load (I_{peak}), is about 0.5 V:

Equation 8

$$R_{SENSE} = \frac{0.5V}{I_{peak}}$$

It should be clear that sensing resistor must absolutely be non-inductive type in order to avoid dangerous negative spikes on SENSE pins. Wire wounded resistors cannot be used here, while metallic film resistors are recommended for their high peak current capability and low inductance. For the same reason the connections between the SENSE pins, C1, C2, V_{SA}, V_{SB} and GND pins (see *Figure 6*) must be taken as short as possible (see *Section 2.4*).

The average power dissipated by the sensing resistor is:

- Fast decay recirculation: $P_R \cong I_{rms}^2 \cdot R_{SENSE}$
- Slow decay recirculation: $P_R \cong I_{rms}^2 \cdot R_{SENSE} \cdot D$

Where D is the duty cycle of the PWM current control, I_{rms} is the RMS value of the load current.

Nevertheless, the sensing resistor power rating should be chosen, taking into account the peak value of the dissipated power:

Equation 9

$$P_R \cong I_{pk}^2 \cdot R_{SENSE}$$

Where I_{pk} is the peak value of the load current.

Multiple resistors in parallel help to obtain the required power rating with standard resistors, and reduce the inductance.

The R_{SENSE} tolerance reflects on the peak current error: 1% resistors should be preferred.

Table 1 shows R_{SENSE} recommended values ()for a 0.5 V drops and power ratings for typical RMS and peak current values

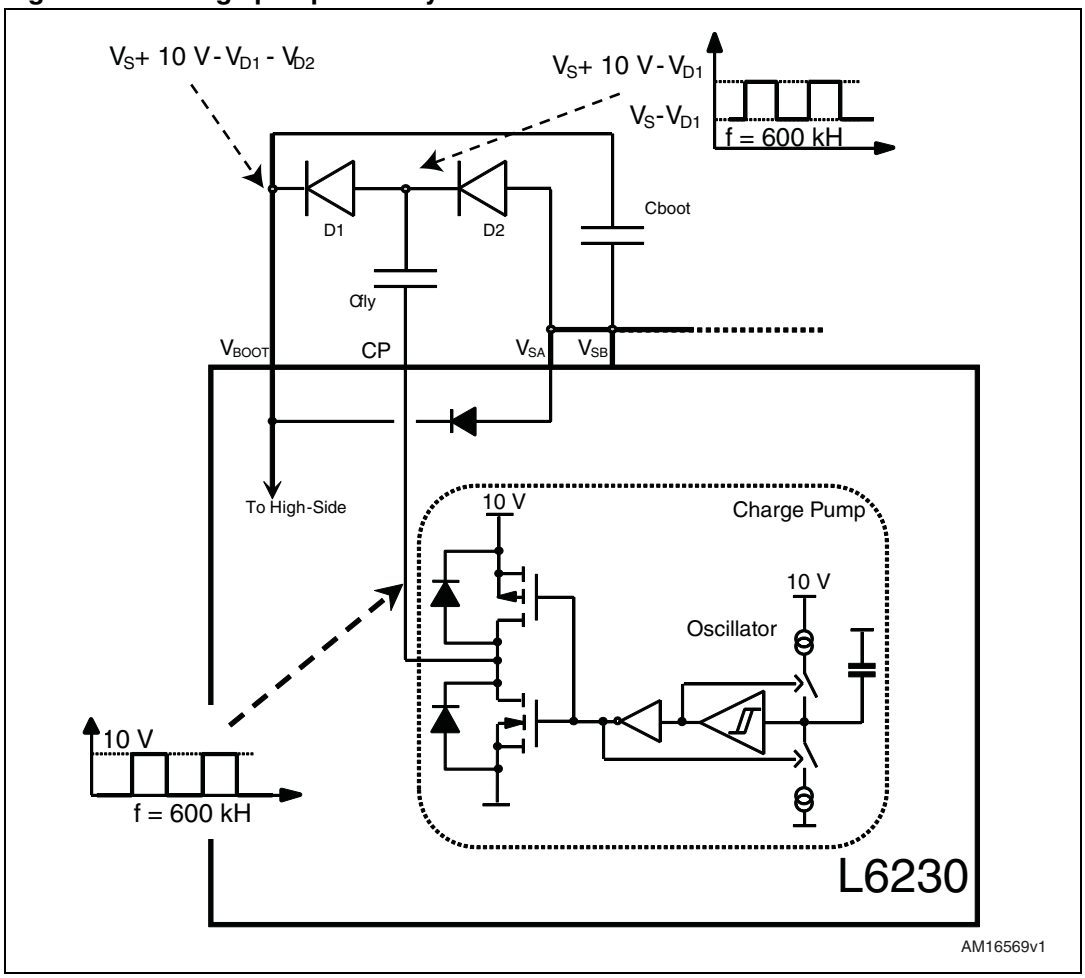
Table 1. R_{SENSE} recommended values

I_{pk} [A]	R_{SENSE} [Ω]	R_{SENSE} power rating [W]	Alternatives
0.25	2	0.125	
0.5	1	0.25	
1	0.5	0.5	2 X 1 Ω 0.25 W paralleled

2.6 Charge pump external components

An internal oscillator, with its output at CP pin, switches from GND to 10 V with a typical frequency of 600 kHz (see *Figure 1*).

Figure 7. Charge pump circuitry



When the oscillator output is at ground, C_{fly} is charged by V_s through D2. When it rises to 10 V, D2 is reverse biased and the charge flows from C_{fly} to C_{boot} through D1, so the V_{BOOT} pin, after some few cycles, reaches the maximum voltage of V_s + 10 V V_{D1} V_{D2}, which supplies the high-side gate drivers.

With a differential voltage between V_S and V_{BOOT} of about 9 V and both the bridges switching at 50 kHz, the typical current drawn by the V_{BOOT} pin is 1.85 mA.

Care must be taken to develop the PCB layout of C_{fly}, D1, D2 connections in order to minimize interferences with the rest of the circuit (see also the *Section 2.4*).

Recommended values for the charge pump circuitry are:

- D1, D2 : 1N4148
- C_{fly} : 10 nF - 100V (ceramic capacitor)
- C_{boot} : 220 nF - 35V (ceramic capacitor)

Due to the high charge pump frequency, fast diodes are required. Connecting the cold side of the bulk capacitor (C2) to V_S instead of GND, the average current in the external diodes during operation is less than 10 mA. At IC power-up the current in the external diodes during operation is less than 200 mA. The reverse voltage is about 10 V in all conditions. The 1N4148 diodes withstand about 200 mA DC (1 A peak), and the maximum reverse voltage is 75 V, so they should fit for the majority of applications.

2.7 Sharing the charge pump circuitry

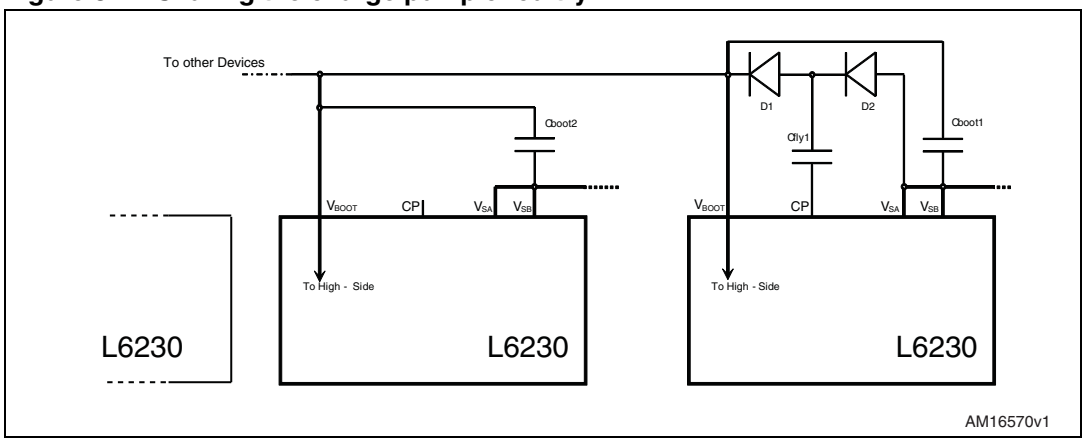
If more than one device is used in the application, it is possible to use the charge pump from one L6230 to supply the V_{BOOT} pins of several ICs. The unused CP pins on the slave devices are left unconnected, as shown in *Figure 8*. A 100 nF capacitor (C_{boot2}) should be connected to the V_{BOOT} pin of each device. Supply voltage pins (V_S) of the devices sharing charge pump must be connected together.

The higher the number of devices sharing the same charge pump, the lower the differential voltage available for gate drive (V_{BOOT} - V_S), causing a higher $R_{DS(on)}$ for the high-side DMOS, so higher dissipating power.

A better performance can also be obtained using a 33 nF capacitor for C_{fly} and using Schottky diodes (for example BAT47 are recommended).

Sharing the same charge pump circuitry for more than 3 or 4 devices is not recommended, since it reduces the V_{BOOT} voltage increasing the high-side MOS on-resistance and thus power dissipation.

Figure 8. Sharing the charge pump circuitry



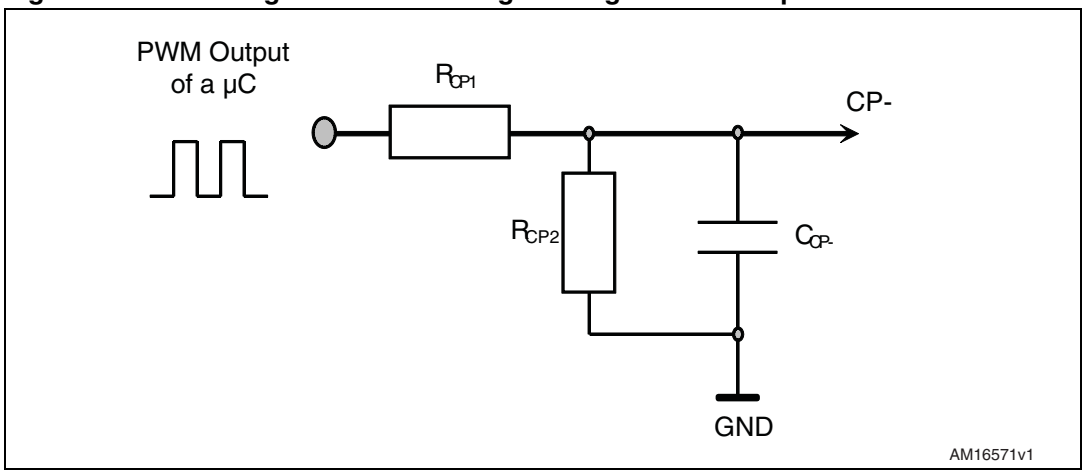
2.8 How to generate a reference voltage for the current control

The device has an analog input (CP-) connected to the internal comparator, that can be used to control the peak value of the motor current through an external control loop.

A fixed reference voltage can be easily obtained with a resistive divider from an available pull-up voltage rail (maybe the one supplying the microcontroller or the rest of the application) and GND.

A very simple way to obtain a variable voltage without using a DAC is to low-pass filter a PWM output of a µC (*Figure 9*).

Figure 9. Obtaining a reference voltage through a PWM output of microcontroller



Assuming that this output swings from 0 to 5V, the resulting average voltage is:

Equation 10

$$V_{CP-} = \frac{5V \cdot D_{\mu C} \cdot R_{CP2}}{R_{CP1} + R_{CP2}}$$

where DµC is the duty cycle of the PWM output of the microcontroller.

Assuming that the microcontroller output impedance is lower than 1 kΩ, with R_{CP1} = 5.6 kΩ, R_{CP2} = 1.5 k, C_{CP} = 100 nF and a PWM switching from 0 to 5 V at 100 kHz, the low-pass filter time constant is about 0.12 ms and the remaining ripple on the V_{CP-} voltage is about 20 mV. Higher values for R_{CP1}, R_{CP2} and C_{CP} reduce the ripple, but the reference voltage takes more time to vary after changing the duty cycle of the microcontroller PWM. Besides, too high values of R_{CP1} also increase the impedance of the CP- net at low frequencies, causing a poor noise immunity.

As sensing resistor value is typically kept small, a small noise on CP- input pins might cause a considerable error in the output current. It is then recommended to decouple this pin with a ceramic capacitor of some tens of nF, placed very close to CP- and GND pins.

Note that CP- pin connected to GND cannot guarantee zero current due to voltage offset in the internal comparator. The best way to cut down the IC power consumption and to clear the load current is to pull down the DIAG/EN pin.

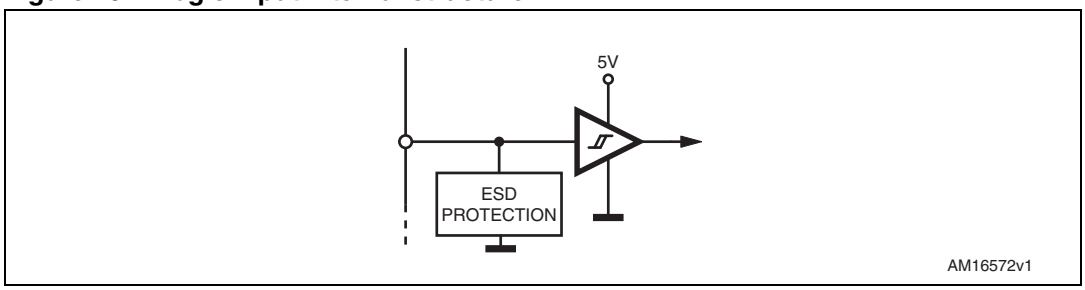
With very small reference voltage, PWM current control method can lose control of the current due to the minimum allowed duration of on-time.

2.9 Input logic pins

INx and ENx pins are TTL/CMOS and microcontroller compatible logic input pins. The internal structure is shown in *Figure 10* . Typical values for turn-on and turn-off thresholds are $V_{TH(ON)}$ = 1.8 V and $V_{TH(OFF)}$ = 1.3 V.

Pins are ESD protected and can be directly connected to the logic outputs of a microcontroller; a series resistor is generally not recommended, as it could help inducted noise to disturb the inputs.

Figure 10. Logic input internal structure



DIAG-EN pin has the same input structure with the exception that the drain of the overcurrent and MOSFET thermal protection is also connected to this pin. Due to this connection, this pin has to be driven very carefully. The EN input may be driven in one of two configurations as shown in *Figure 11* or *Figure 12*. If driven by an open-drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in *Figure 11*. If the driver is a standard push-pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in *Figure 12*. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ Recommended values for R_{EN} and C_{EN} are respectively 10 kΩ and 5.6 nF.

More information on selecting the values is found in *Section 2.10*.

Figure 11. Pin DIAG/EN open collector driving

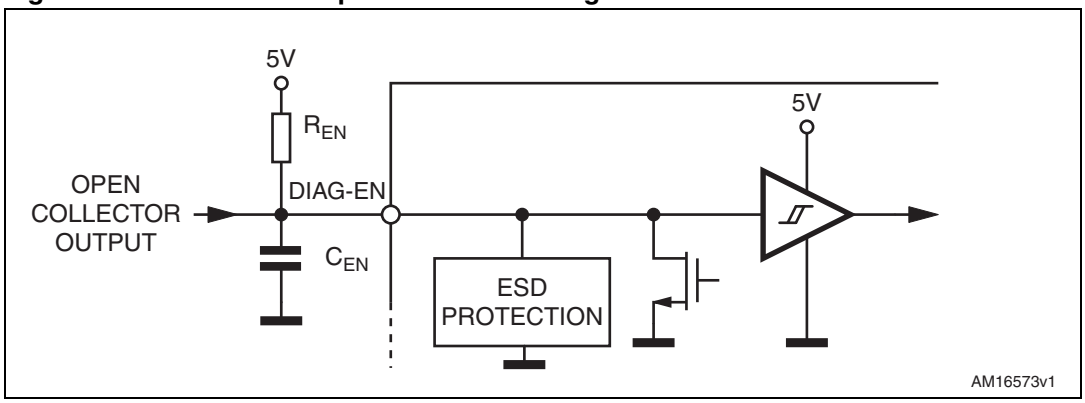
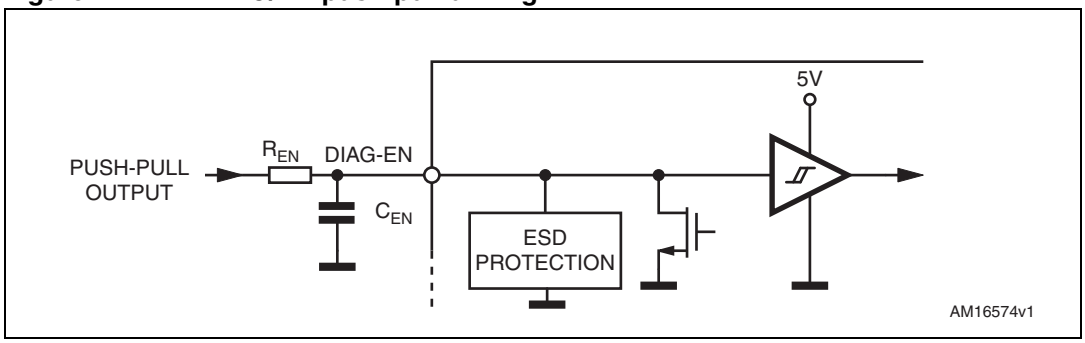


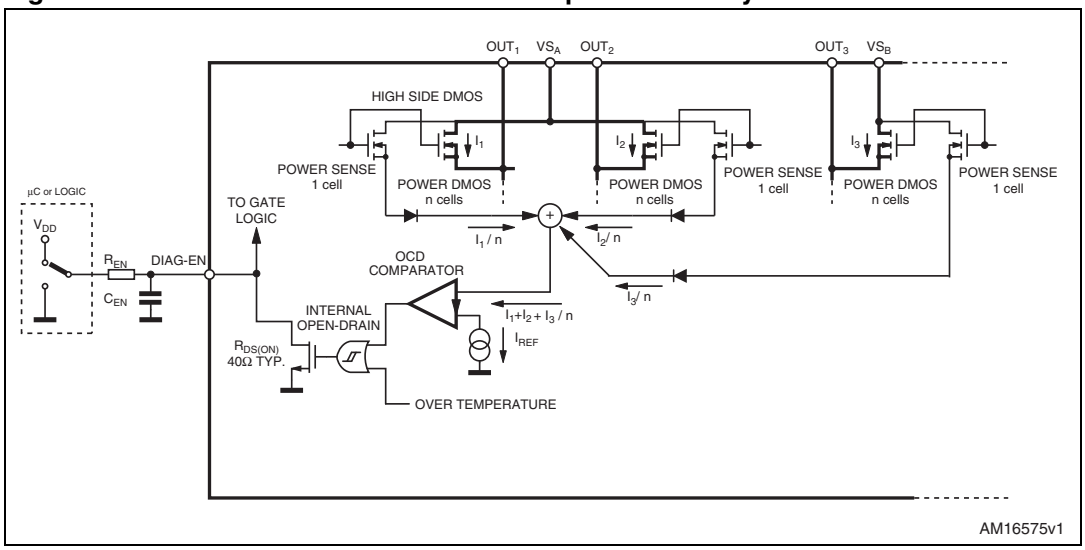
Figure 12. Pin DIAG/EN push-pull driving



2.10 Overcurrent protection

To implement an overcurrent protection, a dedicated overcurrent detection (OCD) circuitry (see *Figure 13* for a simplified schematic) senses the current in each high-side. Power DMOS are actually made of thousands of individual identical cells, each carrying a fraction of the total current flowing. The current sensing element, connected in parallel to the power DMOS, is made of only a few cells, having a 1:N ratio compared to the power DMOS. The total drain current is split between the output and the sense element according to the cell ratio. Sensed current is, then, a small fraction of the output current and does not contribute significantly to power dissipation.

Figure 13. L6230 overcurrent detection simplified circuitry



This sensed current is compared to an internally-generated reference to detect an overcurrent condition. An internal open-drain MOSFET turns on when the sum of the currents in the bridge 1, the bridge 2 or the bridge 3 reaches the threshold (2.8 A typical value); the open-drain is available at the DIAG-EN pin for diagnostic purposes and to ensure an overcurrent protection, connecting an RC network (see *Figure 13*).

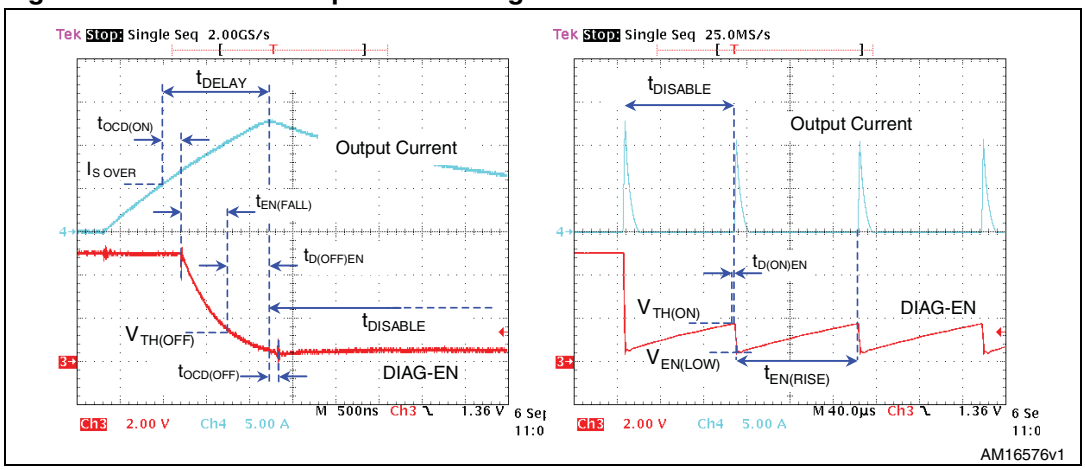
Figure 14 shows the device operating in overcurrent condition.

When an overcurrent is detected the internal open-drain MOSFET pulls the DIAG-EN pin to GND, switching off all 6 power DMOS of the device and allowing the current to decay. Under a persistent overcurrent condition, like a short to ground or a short between two output pins, the external RC network on the EN pin (see *Figure 13*) reduces the RMS value of the output current by imposing a fixed disable time after each overcurrent occurrence.

The values of R_{EN} and C_{EN} are selected to ensure proper operation of the device under a short-circuit condition. When the current flowing through the high-side DMOS reaches the OCD threshold (2.8 A typ.), after an internal propagation delay ($t_{OCD(ON)}$) the open-drain starts discharging C_{EN}. When the DIAG-EN pin voltage falls below the turn-off threshold ($V_{TH(OFF)}$) all the Power DMOS turn off after the internal propagation delay ($t_{D(OFF)EN}$). The current begins decaying as it circulates through the freewheeling diodes. Since the DMOS are off, there is no current flowing through them and no current to sense so the OCD circuit, after a short delay ($t_{OCD(OFF)}$), switches the internal open-drain device off, and R_{EN} can charge C_{EN}. When the voltage at DIAG-EN pin reaches the turn-on threshold ($V_{TH(ON)}$), after the $t_{D(ON)EN}$ delay, the DMOS turn on and the current restarts.

Even if the maximum output current can be very high, the external RC network provides a disable time ($t_{DISABLE}$) to ensure a safe RMS value (see *Figure 14*).

Figure 14. Overcurrent operation timing



The maximum value reached by the current depends on its slew-rate, thus on the state of short-circuit, the supply voltage, and on the total intervention delay (t_{DELAY}). It can be noticed that after the first current peak, the maximum value reached by the output current becomes lower, because the capacitor on DIAG-EN pins is discharged starting from a lower voltage, resulting in a shorter t_{DELAY}.

The following approximate relations estimate the disable time and the first OCD intervention delay after the short-circuit (worst case).

The time the device remains disabled is:

Equation 11

$$t_{DISABLE} = t_{OCD(OFF)} + t_{EN(RISE)} + t_{D(ON)EN}$$

where

Equation 12

$$t_{EN(RISE)} = R_{EN} \cdot C_{EN} \cdot \ln\frac{V_{DD} - V_{EN(LOW)}}{V_{DD} - V_{TH(ON)}}$$

The total intervention time is:

Equation 13

$$t_{DELAY} = t_{OCD(ON)} + t_{EN(FALL)} + t_{D(OFF)EN}$$

where

Equation 14

$$t_{EN(FALL)} = R_{OPDR} \cdot C_{EN} \cdot \ln\frac{V_{DD}}{V_{TH(OFF)}}$$

$t_{OCD(OFF)}$, $t_{OCD(ON)}$, $t_{D(ON)EN}$, $t_{D(OFF)EN}$, and R_{OPDR} are device intrinsic parameters, V_{DD} is the pull up voltage applied to R_{EN}.

The external RC network, C_{EN} in particular, must be chosen obtaining a reasonable fast OCD intervention (short t_{DELAY}) and a safe disable time (long $t_{DISABLE}$).

Figure 15 shows both $t_{DISABLE}$ and t_{DELAY} as a function of C_{EN}: at least 100µs for $t_{DISABLE}$ are recommended, keeping the delay time about 1 to 2µs at the same time.

Figure 15. Typical disable time vs. C_{EN} (on varying R_{EN})

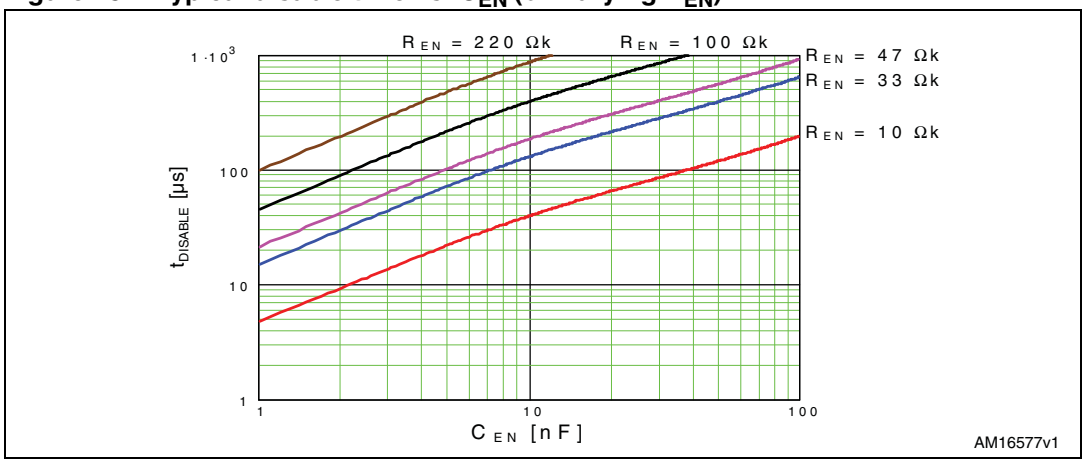
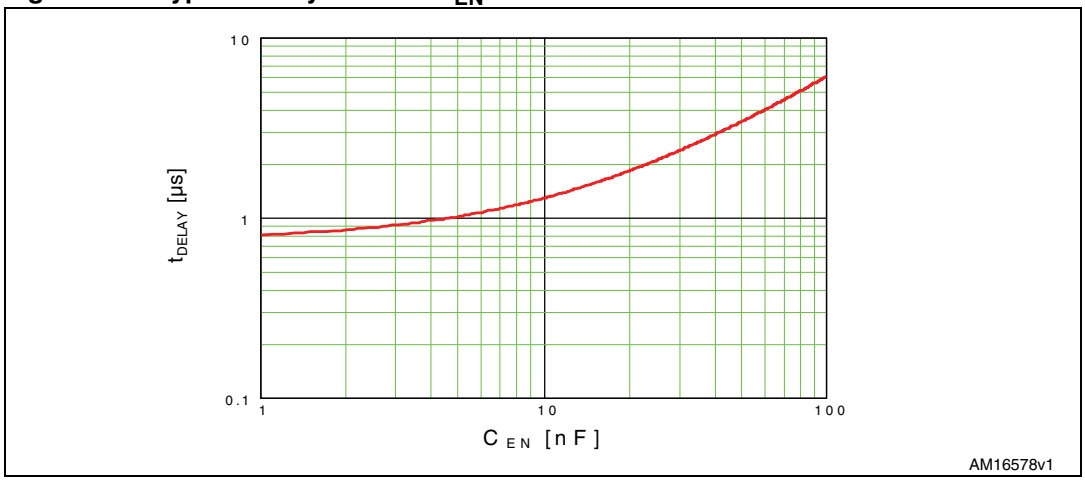


Figure 16. Typical delay time vs. C_{EN}



The internal open-drain can also be turned on if the device experiences an overtemperature (OVT) condition. The OVT causes the device to shut down when the die temperature exceeds the OVT threshold (T_J > 165 °C typ.). Since the OVT is also connected directly to the gate drive circuit (see *Figure 1*), all the power DMOS shut down, even if DIAG-EN pin voltage is still over $V_{th(OFF)}$. When the junction temperature falls below the OVT turn-off threshold (150 °C typ.), the open-drain turns off, C_{EN} is recharged up to $V_{TH(ON)}$ and then the power DMOS are turned back on.

2.11 Thermal management

In most applications, the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides, the available space on the

PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness.

For instance, using a VFQFPN32L 5 x 5 package the typical $R_{th(JA)}$ is about 42 °C/W when mounted on a double-layer FR4 PCB with a dissipating copper area of 0.5 cm_2 on the top side plus 6 cm^2 ground layer connected through 18 via holes (9 below the IC).

Otherwise, using a Power-SO package with copper slug soldered on a 1.5 mm copper thickness FR4 board with 6 cm^2 dissipating footprint (copper thickness of 35 µm), the $R_{th(jA)}$ is about 35 °C/W.

Using a multi-layer board with vias to a ground plane, the thermal impedance can be reduced down to 15 °C/W.

2.12 Brake

In general, motor braking can be achieved making a short-circuit across the windings: the BEMF forces a current, proportional to the braking torque that flows in the opposite direction than in normal running mode. For high BEMF and inertia moment, the current may reach very high values: a power resistor is often used to reduce the maximum braking current and dissipate the motor energy.

In the L6230, brake function can be achieved to quickly stop the motor while it is running: providing a high logic level to the three IN pins all the high-side DMOS switch on, making a short-circuit across the motor windings.

A power resistor is not used: while the motor is braking, both thermal and overcurrent protections still work, avoiding BEMF to cause a current exceeding the device's maximum ratings. Using a RC network (see *Section 2.10*) a disable time between each overcurrent event can be set, reducing the maximum RMS value of the current.

Figure 17 shows what happens if the current exceeds the OCD threshold while the motor is braking: as soon as the current, in one of the three motor phases, reaches the OCD threshold (2.8 A typ.), the open-drain MOSFET internally connected to the DIAG-EN pin discharges the external capacitor; the DIAG-EN pin voltage falls to GND and all the bridges of the device are disabled for a time that depends on the RC network values. During this disable time, the current, forced by the BEMF decreases and so the braking torque; when the current becomes zero (because the motor inductances have been fully discharged), if the BEMF is less than the supply voltage there is no braking effect (since the freewheeling diodes cannot be turned on) until the disable time expires and all the high-side power DMOS turn on again.

Figure 17. Example of overcurrent during motor braking

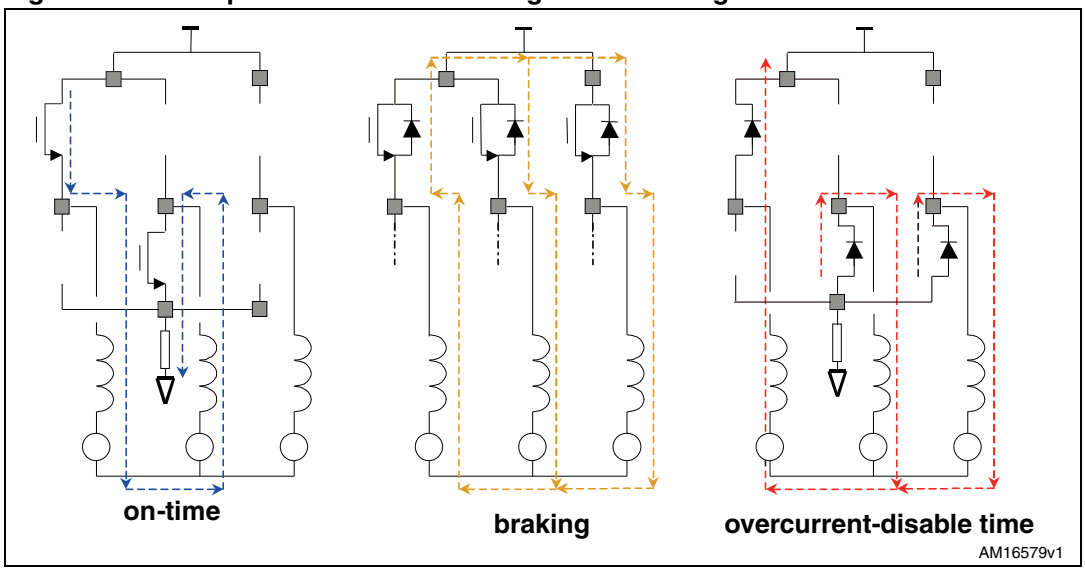
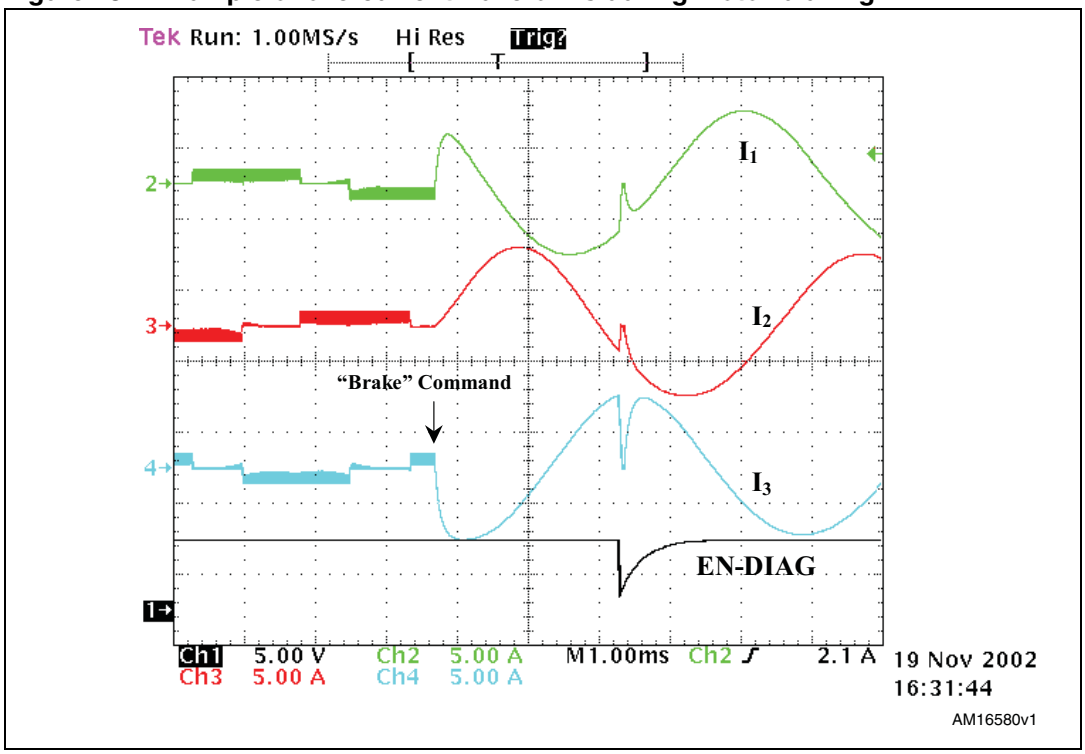


Figure 18. Example of overcurrent waveforms during motor braking



3 Application information

Here below some general suggestions for applications based on the L6230 three-phase BLDC motor driver.

A high quality ceramic capacitor (C_2) in the range of 100 nF to 200 nF should be placed between the power pins V_{SA} and V_{SB} and ground near the L6230 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching.

The capacitor (C_{EN}) and resistor (R_{EN}) connected between the DIAG-EN input and ground set the delay time and disable time when an overcurrent is detected (see *Section 2.10*).

The current sensing inputs ($SENSE_X$) should be connected to the sensing resistors R_{SENSE} with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the dI/dt transients across the resistors.

To increase noise immunity, unused logic pins are connected either to 5 V (high logic level) or GND (low logic level).

The power ground and signal ground have to be kept separated on PCB.

In *Table 2*, recommended values are reported for external components.

Table 2. Component values for typical applications

Component	Value	Description
C_1	100 µF	Bulk capacitor
C_2	100 nF	Supply voltage ceramic capacitor (one for V_S pins)
C_{BOOT}	220 nF	Bootstrap capacitor connected between V_{BOOT} and V_S (charge pump)
C_{EN}	5.6 nF	Capacitor connected to DIAG-EN pin
C_P	10 nF	Fly capacitor connected to CP pin (charge pump)
D_1	1N4148	Charge pump diode
D_2	1N4148	Charge pump diode
R_{EN}	100 kΩ	Resistor connected to DIAG-EN pin

3.1 Field oriented control driving method

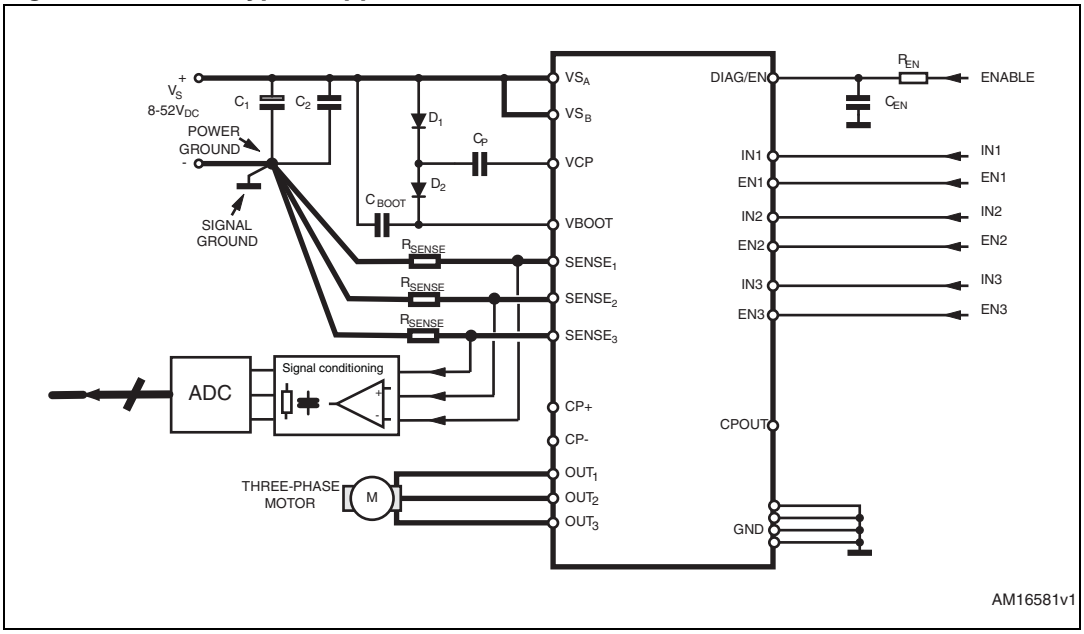
The field oriented control (F.O.C.) method allows smooth and precise motor control of BLDC motors to be provided. In this configuration (see *Figure 19*), three sensing resistors are required, one for each channel.

The sensing signals, coming from the output power stage, are conditioned by external operational amplifiers which provide the proper feedback signals to the analog-to-digital converter and the system controller. According to the feedback signals the six input lines are generated by the controller.

Note that some filtering and level shifting RC networks should be added between the sense resistor and the correspondent op-amp input.

The uncommitted internal comparator with open-drain output is available.

Figure 19. F.O.C. typical application



3.2 Six-step driving method with current control

The input sequence is generated by the external controller and the L6230 comparator is used to obtain the information for the peak current control. In this configuration, only one sense resistor is needed, the three OUT pins are connected together to R_{SENSE} (see *Figure 20*).

The non-inverting input comparator CP+ monitors the voltage drop across the external sense resistor connected between the source of the three lower power MOS transistors and ground.

As the current in the motor increases the voltage across, the R_{SENSE} increases proportionally. When the voltage drop across, the sense resistor becomes greater than the reference voltage applied to inverting input CP- the comparator open-drain output is switched on pulling down the CPOUT pin.

This signal could be managed by controller to generate the proper input sequence for six-step driving method with current control and select what current decay method to implement.

When the sense voltage decreases below the CP- voltage, the open-drain is switched off and the voltage at CPOUT pin increases charging the capacitor C_3.

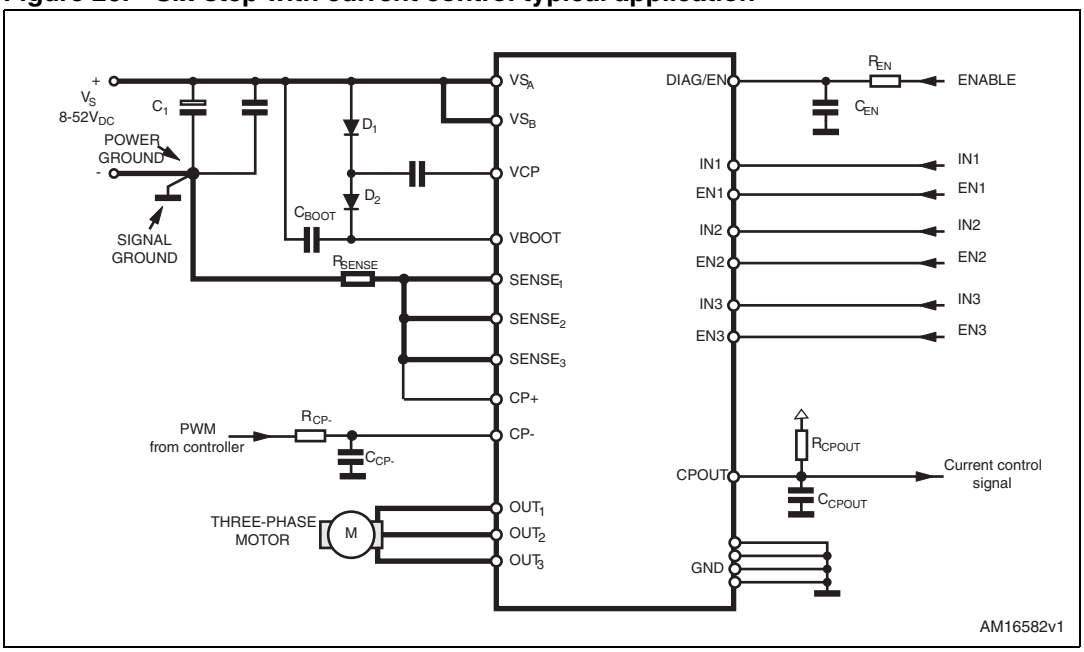
The reference voltage at pin CP- is set according to the sense resistor value and the desired regulated current:

Equation 15

$$V_{CP-} \cong R_{SENSE} \times I_{TARGET}$$

A very simple way to obtain a variable voltage is to low-pass filter a PWM output of a controller (refer to *Section 2.8*).

Figure 20. Six-step with current control typical application



3.3 Six-step driving method with BEMF zero crossing detection

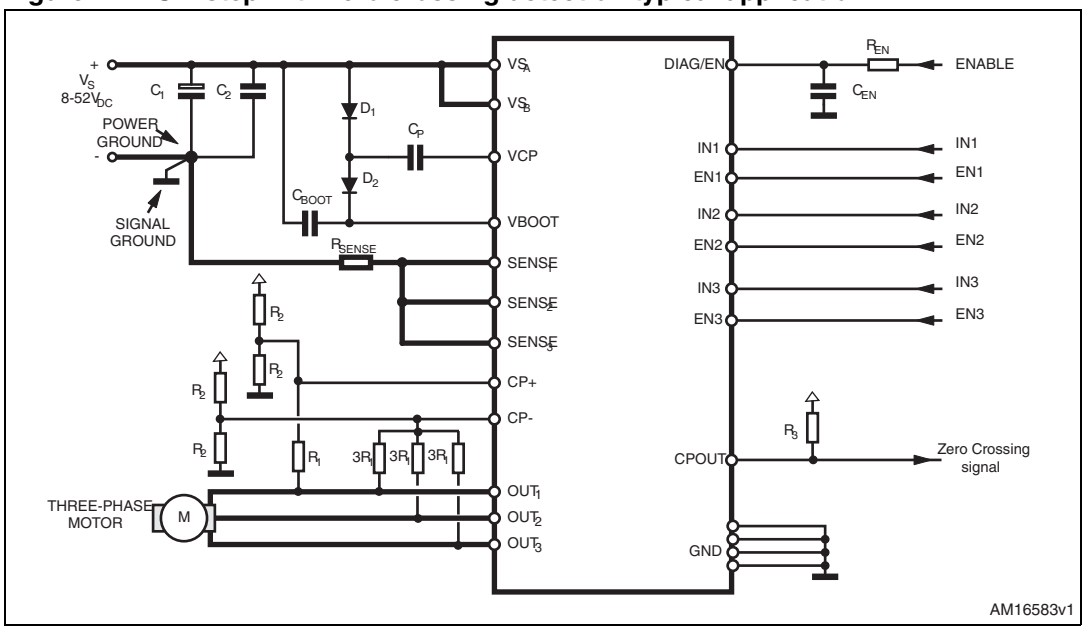
To implement a sensorless motor control system, the information on rotor position is achieved by BEMF zero-crossing detection; in this way, no hall-effect sensors or encoders are needed.

In six-step driving mode one of the three phases is left in high-impedance state. Comparing the voltage of this phase with the motor neutral point voltage (or star point) we can detect the BEMF zero-crossing. This information about the commutation between two consecutive steps allows the rotor synchronization to be achieved.

In the example of *Figure 21*, the OUT1 phase voltage is monitored by the CP+; the center-tap voltage is obtained as combination of three phase voltages and monitored by the CP- pin (R_2 >> R_1). Only when the OUT1 is in high-impedance, the CPOUT performs a commutation each time a BEMF zero crossing is detected.

In this configuration one sense resistor is needed, the three OUT pins are connected together to R_{SENSE}.

Figure 21. Six-step with zero crossing detection typical application



4 Demonstration boards

4.1 EVAL6230QR demonstration board

A demonstration board has been produced to help the evaluation of the device in VFQFPN32L 5 x 5 mm package.

It implements a typical application which can be used as a reference design to drive three-phase brushless DC motors with currents up to 1 A DC.

Thanks to the small footprint of the L6230Q the PCB is very compact (32 x 31 mm).

For more details on the EVAL6230QR, refer to the application note AN3244.

Figure 22. Demonstration board

4.2 STEVAL-IFN003V1:PMSM FOC motor driver based on the L6230 and STM32F103

The STEVAL-IFN003V1 demonstration board is based on the DMOS fully integrated three-phase motor driver L6230 and STMicroelectronics' ARM™ Cortex-M3 core-based STM32F103 microcontroller implementing field-oriented control of a PMSM motor.

The board is designed as an evaluation environment for motor control applications in the range of 8 V - 48 V of DC bus voltage and up to 45 W, exploiting the computational power of the STM32F103.

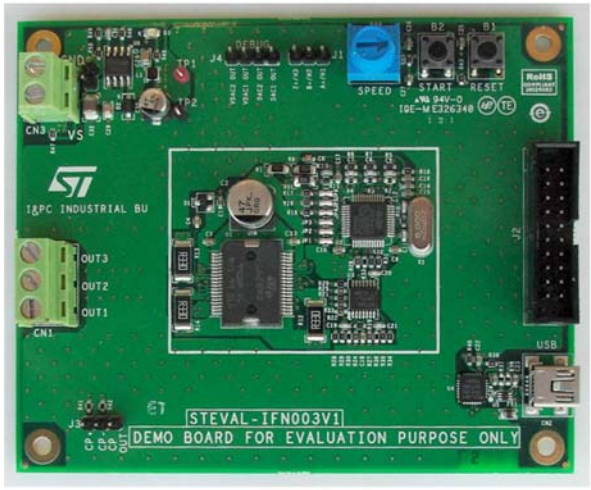
The L6230 DMOS driver features 2.8 A output peak current, non-dissipative overcurrent detection/protection, cross-conduction protection, uncommitted comparator, thermal shutdown and undervoltage lockout.

The STEVAL-IFN003V1 is provided with a specific USB interface for the real-time data exchange.

Offering dedicated hardware evaluation features, the STEVAL-IFN003V1 board is designed to allow developers to evaluate the device and develop their own applications. The STEVAL-IFN003V1 can be used together with the STM32 PMSM single/dual FOC SDK v3.0 and constitutes a complete motor control evaluation and development platform.

For more details on the STEVAL-IFN003V1 refer to the user manual UM1478.

Figure 23. STEVAL-IFN003V1 board



4.3 STEVAL-IFN004V1:BLDC six-step motor driver based on the L6230 and STM8S105

The STEVAL-IFN004V1 demonstration board is based on the DMOS fully integrated three-phase motor driver L6230 and STMicroelectronics' STM8S105 microcontroller implementing 6-step scalar control of a BLDC motor.

The board is designed as an evaluation environment for motor control applications in the range of 8 V - 48 V of DC bus voltage and up to 35 W, exploiting the embedded features of the STM8S105.

The L6230 DMOS driver features 2.8 A output peak current, non-dissipative overcurrent detection/protection, cross-conduction protection, internal comparator used for cycle-by-cycle current limitation/regulation, thermal shutdown and undervoltage lockout.

The STEVAL-IFN004V1 is provided with a specific BEMF detection network with dynamic method selection.

Offering dedicated hardware evaluation features, the STEVAL-IFN004V1 board is designed to help developers evaluate the device and develop their own applications. The STEVAL-IFN004V1 can be used together with the STM8Sxxx three-phase BLDC motor control software library and constitutes a cost-effective complete motor control evaluation and development platform.

For more details on the STEVAL-IFN004V1 refer to the user manual UM1477.

Figure 24. STEVAL-IFN004V1 board

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
29-Jan-2013	1	Initial release.

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